UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/607,815	06/30/2000	Kenneth W. Batcher	72255/02662	2193

23380 7590 07/07/2003

ARTER & HADDEN, LLP
1100 HUNTINGTON BUILDING
925 EUCLID AVENUE
CLEVELAND, OH 44115-1475

EXAMINER
HARKNESS, CHARLES A

ART UNIT	PAPER NUMBER
2183	2

DATE MAILED: 07/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/607,815	BATCHER, KENNETH W.	
	Examiner	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Shridhar et al, U.S. Patent Number 5,727,194 (herein referred to as Shridhar).

4. Referring to claim 1 Shridhar has taught a method of operating a processor to repeatedly execute at least one associated instruction, comprising:

loading a register with a count value indicative of the number of times the associated instruction is to be executed (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54);

fetching and executing a REPEAT instruction indicating the at least one associated instruction to be repeatedly executed (Shridhar figures 1,3,4 column 13 line 61-column 14 lines 40, column 15 lines 45-49);

fetching the at least one associated instruction (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54); and

executing the at least one associated instruction for as many times as indicated by the count value (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54).

5. Referring to claim 2 Shridhar has taught a method of operating a processor to repeatedly execute one or more instructions, comprising:

fetching a REPEAT instruction (Shridhar figures 1,3,4 column 13 line 61-column 14 lines 40, column 15 lines 45-49);

executing a REPEAT instruction, wherein execution of the REPEAT instruction stores in a register a count value indicative of the number of tunes one or more associated instructions are be executed(Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54 column 18 lines 5-46);

fetching the one or more associated instructions; and executing the associated instruction for as many times as indicated by the count value (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54).

6. Referring to claim 3 Shridhar has taught a method of operating a processor to repeatedly execute one or more instructions, comprising:

loading a register with a count value indicative of the number of times one or more associated instructions are to be executed (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54 column 18 lines 5-46 column 15 lines 45-49);

fetching and executing a REPEAT instruction indicating the one or more associated instructions that are to be repeatedly executed (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54 column 18 lines 5-46 column 15 lines 45-49);

incrementing a program counter (Shridhar column 15 lines 9-11 column 16 lines 15-20);

fetching the one or, more associated instructions (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54 column 18 lines 5-46 column 15 lines 45-49); and

executing the one or more associated instruction for as many times as indicated by a count value stored in a count register (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54 column 18 lines 5-46 column 15 lines 45-49).

7. Referring to claim 4 Shridhar has taught wherein said count value is stored in said count register before execution of said REPEAT instruction (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54 column 18 lines 5-46 column 15 lines 45-49; since the decode stage come before the fetch stage, as shown in figure 1, the information would be passed in the repeat circuitry before the repeat instruction was executed).

8. Referring to claim 5 Shridhar has taught wherein said REPEAT instruction includes the count value that is stored in said count register, wherein execution of the REPEAT instruction stores the count value in said count register (Shridhar figures 1,3,4 column 13 lines 61-67, column 14 lines 32-54 column 18 lines 5-46 column 15 lines 45-49).

9. Referring to claim 6 Shridhar has taught wherein said method further comprises: incrementing the program counter after the one or more associated instructions have been executed for as many times as indicated by the count value (Shridhar column 15 lines 9-11

column 16 lines 15-20 column 18 lines 13-15; the program would have to increment to the next address that it can continue executing the program outside of the loop).

10. Referring to claim 7 Shridhar has taught wherein method further comprises: decrementing said count value stored in said register each time said one or more associated instructions are executed; and determining whether said count value is less than or equal to zero (Shridhar column 18 lines 31-38).

11. Claims 8-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Kiuchi et al, U.S. Patent Number 5,579,493 (herein referred to as Kiuchi).

12. Referring to claim 8 Kiuchi has taught a processor for repeatedly execute at least one associated instructio11, said processor comprising:

load means for loading a register with a count value indicative of the number of times the associated instruction is to be executed (Kiuchi column 7 lines 18-31; there be required some loading means for the count to get into the correct register);

first fetch means for a REPEAT instruction indicating the at least one associated instruction to be repeatedly executed (Kiuchi figure 1 reference numbers 106,119; sends the signal to the program memory to show to get the repeat instruction);

first execute means for executing the REPEAT instruction indicating the at least one associated instruction to be repeatedly executed (Kiuchi figure 1 reference numbers 104,105);

second fetch means for fetching the at least one associated instruction (Kiuchi figure 2 reference number 122,201; once repeating the instructions, the signal is sent out from 122,201 column 9 lines 18-26 figure 2 reference number 114,216 and 206; sends the signal to the selector in figure 1); and

first execute means for executing the at least one associated instruction for as many times as indicated by the count value (Kiuchi figure 1 reference numbers 104,105).

13. Referring to claim 9 Kiuchi has taught a processor for repeatedly executing one or more instructions, comprising:

first fetch means for fetching a REPEAT instruction (Kiuchi figure 1 reference numbers 106,119; sends the signal to the program memory to show to get the repeat instruction);

first execute means for executing a REPEAT instruction, wherein execution of the REPEAT instruction stores in a register a count value indicative of the number of times one or more associated instructions are be executed (Kiuchi figure 1 reference numbers 104,105; figure 1 reference numbers 106,119; sends the signal to the program memory to show to get the repeat instruction);

second fetch means for fetching the one or more associated instructions (Kiuchi figure 2 reference number 122,201; once repeating the instructions, the signal is sent out from 122,201 column 9 lines 18-26 figure 2 reference number 114,216 and 206; sends the signal to the selector in figure 1); and

second execute means for executing the associated instruction for as many times as indicated by the count value (Kiuchi figure 2; the execution means in figure 2 makes sure the associated instructions are executed for as many times as indicated in the count register).

14. Referring to claim 10 Kiuchi has taught a processor for repeatedly executing one or more instructions, comprising:

load means for loading a register with a count value indicative of the number of times one or more associated instructions are to be executed (Kiuchi column 7 lines 18-31; there be required some loading means for the count to get into the correct register);

first fetch means for fetching a REPEAT instruction indicating the one or more associated instructions that are to be repeatedly executed; (Kiuchi figure 1 reference numbers 106,119; sends the signal to the program memory to show to get the repeat instruction);

first execute mean for executing the REPEAT instruction indicating the one or more associated instructions that are to be repeatedly executed (Kiuchi figure 1 reference numbers 104,105; figure 1 reference numbers 106,119; sends the signal to the program memory to show to get the repeat instruction);

means for incrementing a program counter (Kiuchi figure 1 reference numbers 104,105; figure 1 reference numbers 106,119; sends the signal to the program memory to show to get the repeat instruction; the PC would have to be incremented, if not properly incremented, then the program would only fetch one instruction);

second fetch means for fetching the one or more associated instructions (Kiuchi figure 2 reference number 122,201; once repeating the instructions, the signal is sent out from 122,201 column 9 lines 18-26 figure 2 reference number 114,216 and 206; sends the signal to the selector in figure 1); and

second execute means for executing the one or more associated instruction for as many times as indicated by a count value stored in a count register (Kiuchi figure 2; the execution means in figure 2 makes sure the associated instructions are executed for as many times as indicated in the count register).

15. Referring to claim 11 Kiuchi has taught wherein said count value is stored in said count register before execution of said REPEAT instruction (Kiuchi column 3 lines 38-56 column 2 lines 55-58; figure 1 reference numbers 104,105, since the information for the instruction is sent over the repeat control circuit from the decoder, the count will be stored before the repeat instruction is sent to the execution unit).

16. Referring to claim 12 Kiuchi has taught wherein said REPEAT instruction includes the count value that is stored in said count register, wherein execution of the REPEAT instruction stores the count value in said count register (Kiuchi column 3 lines 38-56 column 2 lines 55-58).

17. Referring to claim 13 Kiuchi has taught wherein said processor further comprises: means for incrementing the program counter after the one or more associated instructions have been executed for as many times as indicated by the count value (Kiuchi column 5 lines 37-42; the PC would have to be incremented after the repeat process was completed, otherwise it would not continue to execute other instructions in the program).

18. Referring to claim 14 Kiuchi has taught wherein processor further comprises:

means for decrementing said count value stored in said register each time said one or more associated instructions are executed; and

means for determining whether said count value is less than or equal to zero Kiuchi column 7 lines 33-44).

19. Referring to claim 15 Kiuchi has taught a processor for repeatedly executing one or more processor instructions, said processor comprising:

a memory address register associated with a main memory (Kiuchi column 8 lines 46-50);

a memory data register associated with the main memory (Kiuchi column 2 lines 30-36);

a memory control for generating memory control signals (Kiuchi column 3 lines 38-56);

a program counter for storing a memory address location of the main memory where an instruction is to be fetched (Kiuchi figure 1 reference number 106 column 5 lines 37-56);

an instruction register for storing an instruction that is to be executed (Kiuchi column 3 lines 9-22);

at least one general purpose register (Kiuchi column 12 lines 13-20; a register file);

decode and execute control logic for decoding and executing an instruction stored in the instruction register (Kiuchi figure 1 reference numbers 104,105 column 5 lines 37-56); and

a state machine for controlling the fetching and repeated execution of one or more associated instructions (Kiuchi column 6 lines 46-64; shows the different state the machine goes to implying a state machine).

20. Referring to claim 16 Kiuchi has taught wherein said processor further comprises an instruction buffer for storing the one or more associated instructions (Kiuchi figure 1 reference number 108).

21. Referring to claim 17 Kiuchi has taught wherein said general purpose register includes a first register for storing a count value indicative of the number of times the one or more associated instructions are to be repeatedly executed (Kiuchi figure 2 reference number 207 column 7 lines 18-31).

22. Referring to claim 18 Kiuchi has taught wherein said state machine generates signals for decrementing the count value stored in the first register (Kiuchi column 7 lines 33-44).

23. Referring to claim 19 Kiuchi has taught wherein said state machine generates a signal for executing an instruction stored in said instruction register (Kiuchi column 1 lines 42-52; the states would have to have some indication of being ready to execute the instruction).

24. Referring to claim 20 Kiuchi has taught wherein said state machine generate a signal for incrementing said program counter (Kiuchi column 7 lines 18-31; the program counter would be required to be incremented, otherwise only one instruction would ever be fetched for the entire system).

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR 1.111(c).

Boutaud et al U.S. Patent Number 5,907,714, has taught a data processor with repeat instructions and control hardware to execute repeat instructions.

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8:00 A.M. – 5:30 P.M. with every other Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-7579.

Charles Allen Harkness

Examiner

Art Unit 2183

June 29, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100